Memory (DRAM) World in the Next Decade

May 07, 2003

Changhyun Kim

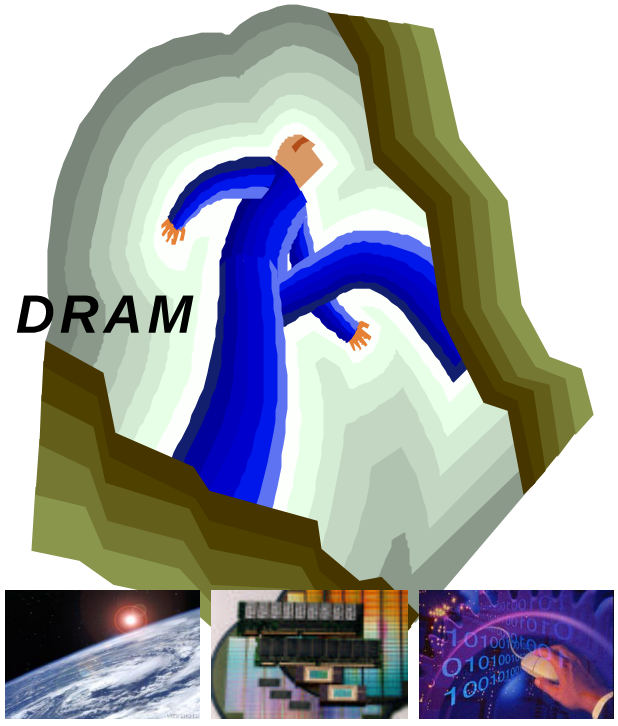
Memory Division
Device Solution Network Business

031-208-6019
Chang.kim@samsung.com

SAMSUNG ELECTRONICS

Contents

1. Introduction
   - MOS Memory
   - State-of-the-art Memory
2. DRAM Introduction & Chip Operation
3. Memory Technology Trend
   - High Density Approach
   - High Speed Approach
   - Low Power Approach
4. Challenges for High Performance DRAM
5. Conclusions



SAMSUNG ELECTRONICS

Semiconductor & Memory

- 도체와 부도체 => 반도체 (Semi-Conductor) 의 매력
  - 원래는 전기가 거의 통하지 않지만 빛이나 열, 또는 불순물을 가해 주면 전기가 통하고 또한 조절이 가능한 물질.

- Memory
  - DRAM, SRAM, NVM

- 사용 단위:
  - Megabit, Mbit= 1024x1024 bit = 1,048,576 bit (백만)
  - Gigabit, Gbit= 1024x1024x1024 bit = 1,073,741,824 bit (십억)

- 대략적 저장 용량
  - 10 Mbit: Book, 1 min CD Audio, 1/4 sec HDTV
  - 1 Gbit: Encyclopedia, 2 hrs CD Audio, 30 sec HDTV

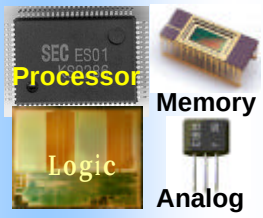
Semiconductor Technology Trend

■ 1950~70's Transistor Era ■ 1980's IC Era ■ 1990's VLSI Era ■ 2000's ULSI/SOC Era

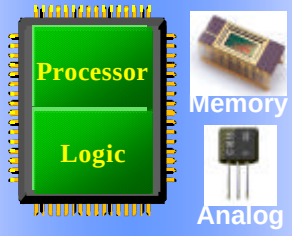
6.0 ~ 3.0um	2.0 ~ 1.0um	0.8 ~ 0.6um	0.5 ~ 0.25um	0.18 ~ 0.13um
1K~64K	256K~4M		16M~128M	256M~1G
8080 ('74)	8086 ('78)	286 ('82)	486 ('89)	Pentium ('93)	Pentium-II ('97)	Pentium III ('98)	Pentium IV ('01)
12V~5V			5V~3.3V	3.3V~1.8V

Transistor

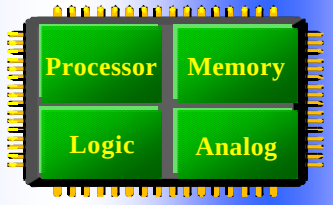
[Discrete]



[Integrated]



[Merged]

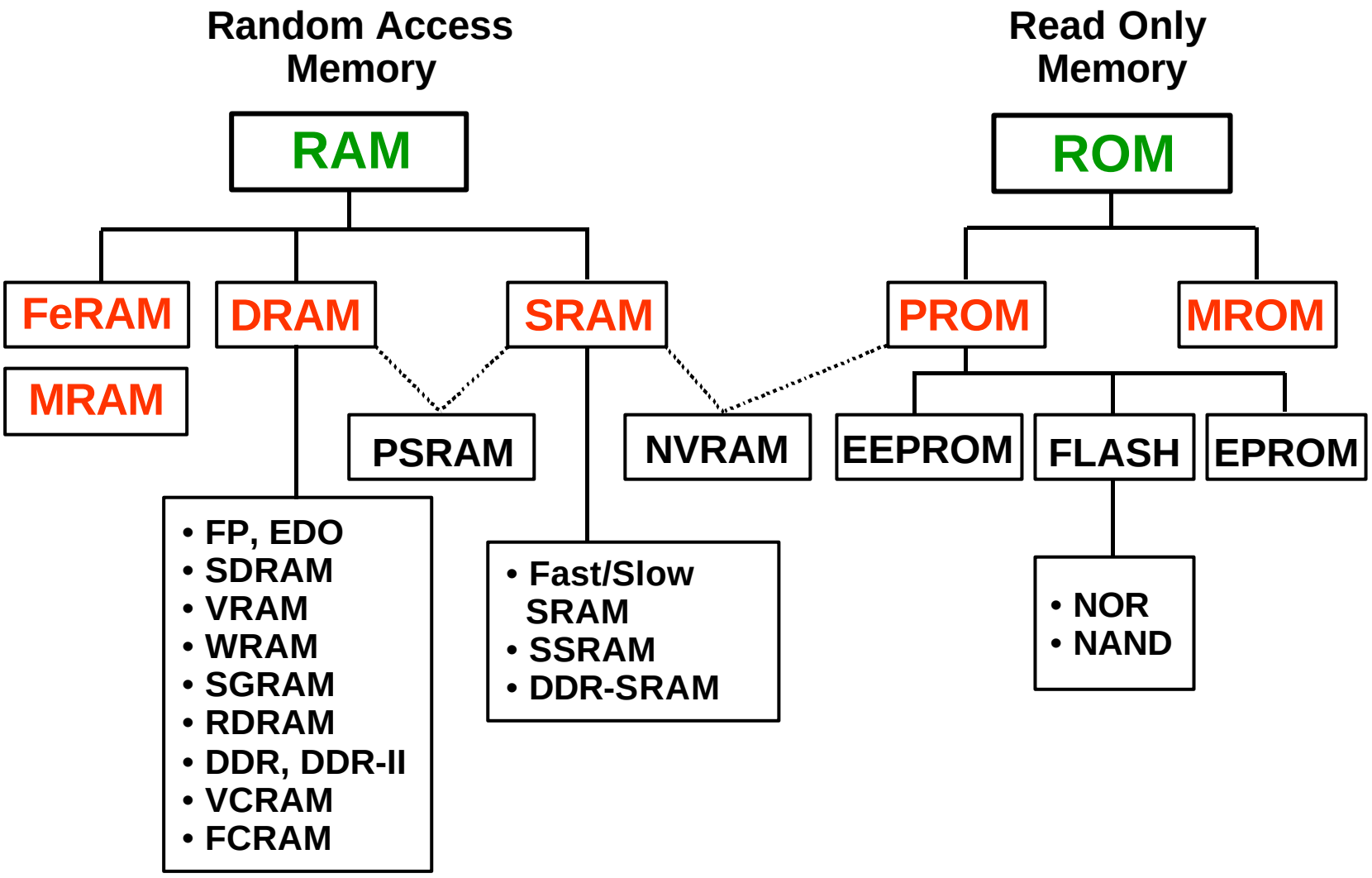


[SOC, Fusion]

SAMSUNG ELECTRONICS

MOS Memory

MOS Memory Tree



SAMSUNG ELECTRONICS

MOS Memory Comparison

- DRAM (Dynamic Random Access Memory)
- SRAM (Static Random Access Memory)
- NVM (Non-Volatile Memory)

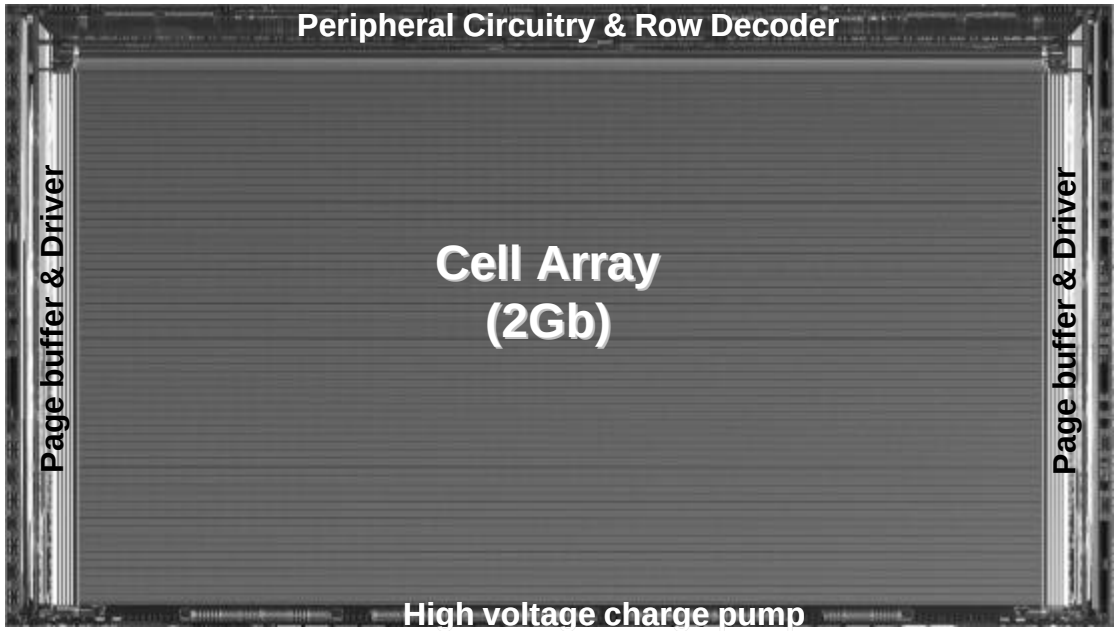
	DRAM	SRAM	NVM
Cell Structure Norm. size	1Tr.+1Cap. 1.0x	6Tr. or 4Tr.+2R 3.0x	1Tr. 0.6x
Power for data Refresh Addressing Density Access speed (Read/Write) Power(standby)	Required Required Multiplexing High 50ns/50ns ~200μA	Required None Non-Mux Low 50ns/50ns (5ns/5ns) 10 μA	None None Non-Mux Very high 50ns/50μs ~10 μA
Application	Main memory, Graphics	Buffer Cache	Bios, Card, File memory

State-of-the-Art Memory

- ***High Density***
- ***High Speed***

0.09um 2Gb NAND Flash (1.45Gb/cm^2)

Highest Bit Density NVM

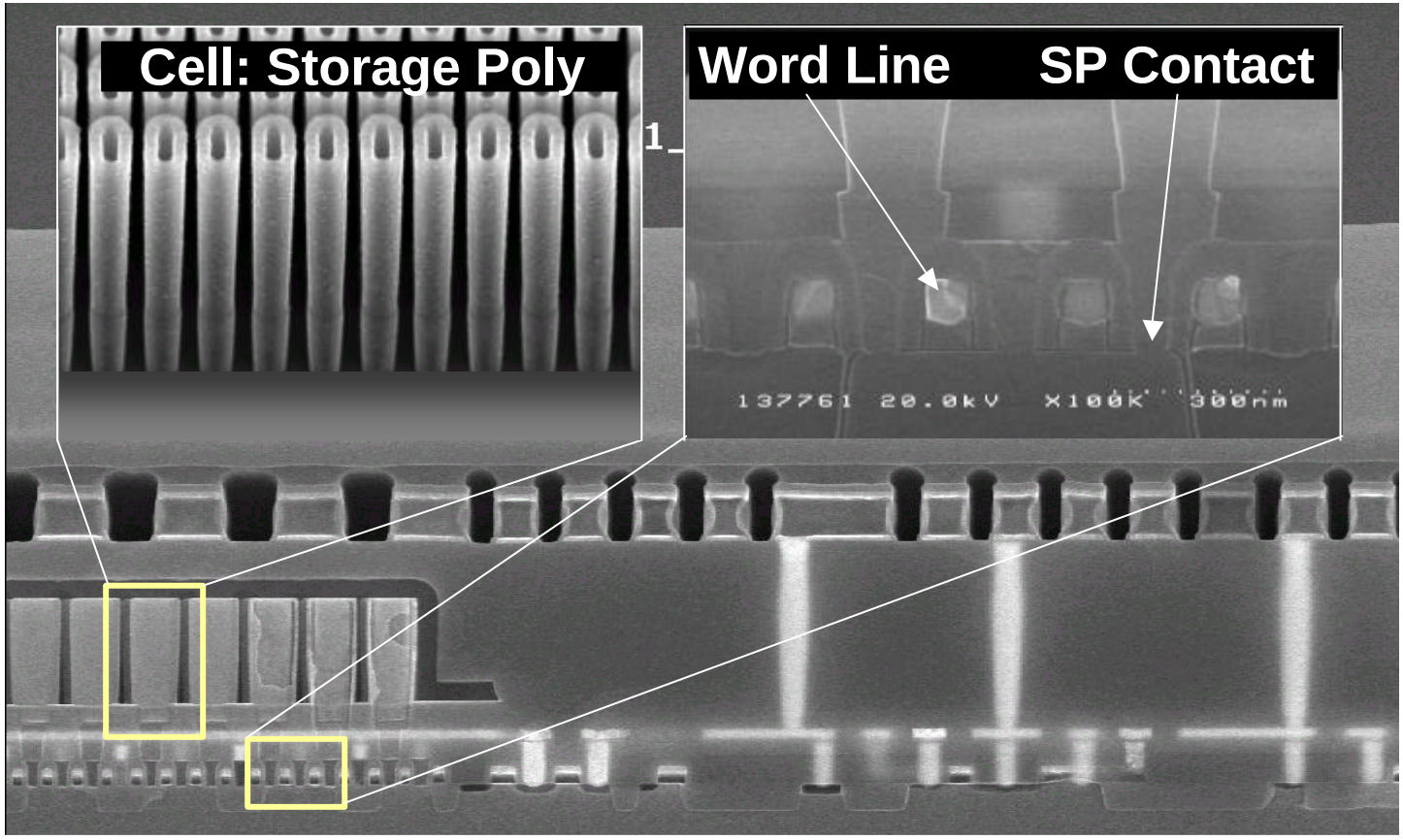


Process Technology	90nm triple-well, 1-W, 1-Al CMOS
Tunnel Oxide	7.0nm
Effective Cell Size	0.044㎟
Chip Size	141mm^2
Block Erase Time	2ms(typ.)
Page Program Time	300ms(typ.)

SAMSUNG ELECTRONICS

0.08um 16Gbit DRAM (1.25Gb/cm²=8Gb/in²)

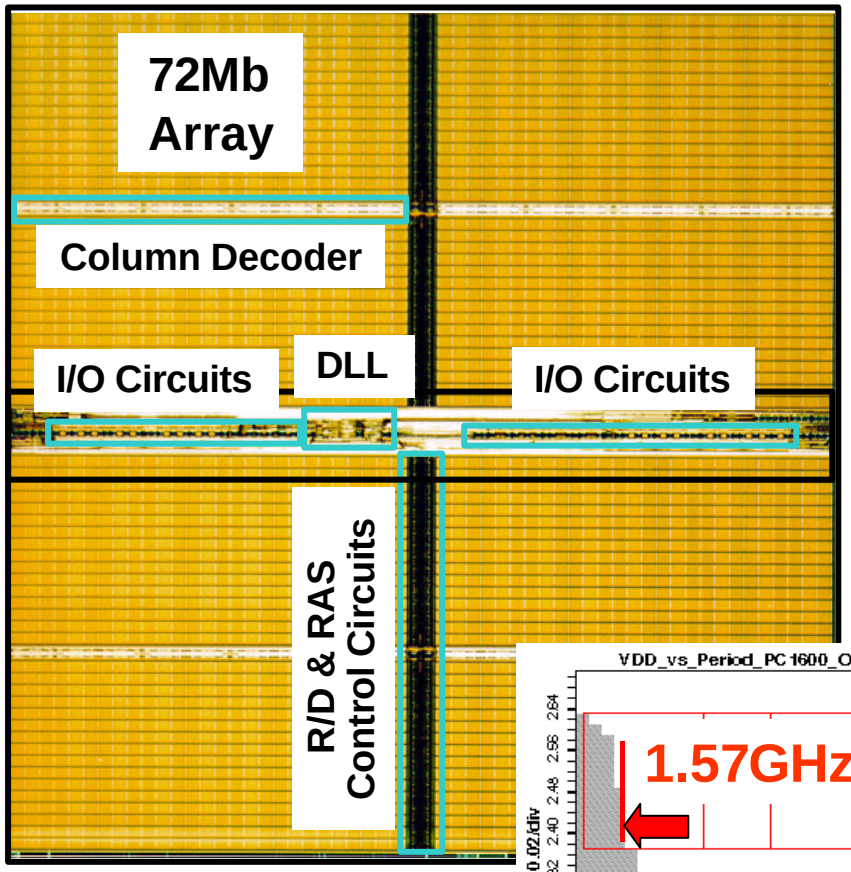
Highest Bit Density DRAM



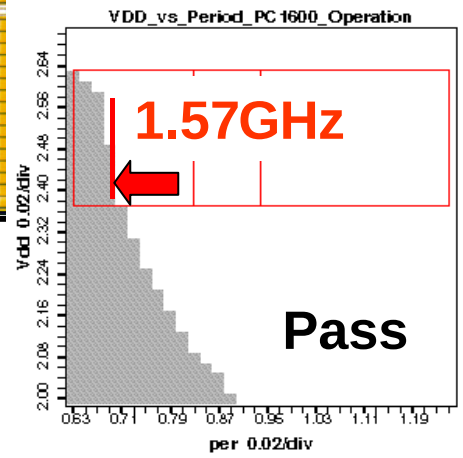
Cell Size = ~0.056㎟

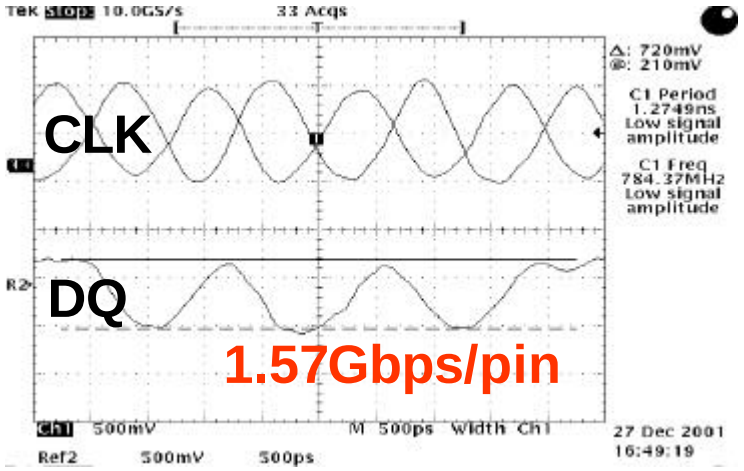
SAMSUNG ELECTRONICS

1.57GHz 576Mb RDRAM



- 0.12㎜, Triple-metal CMOS
- Chip Size = 157.6 mm^2
- V_{CC}/V_{CCA} = 2.5V/2.0V
- 4i Bank, 2KB Page
- Package: 92Ball WBGA





SAMSUNG ELECTRONICS

Present Memory Trend

Memory Density Aspect

- Quadrupled in every three years (Moore's law)
- DRAM: 512Mbit (150 mm^2) ~ 4Gbit (645 mm^2)
  - Bit density = 340~635 $Mbit/cm^2$
- SRAM: 16Mbit (128 mm^2) = 12.5 $Mbit/cm^2$
- NVM: 1Gbit Flash (132 mm^2) ~ 2Gbit (141 mm^2)
  - Bit density = 776~1450 $Mbit/cm^2$
- FRAM: 4Mbit (118 mm^2) => 34 $Mbit/cm^2$

Memory Speed Aspect (Data Transfer Rate)

- DRAM: 100 ~ 800 MHz
- SRAM: 200 ~ 300 MHz
- NVM: 20 ~ 50 MHz

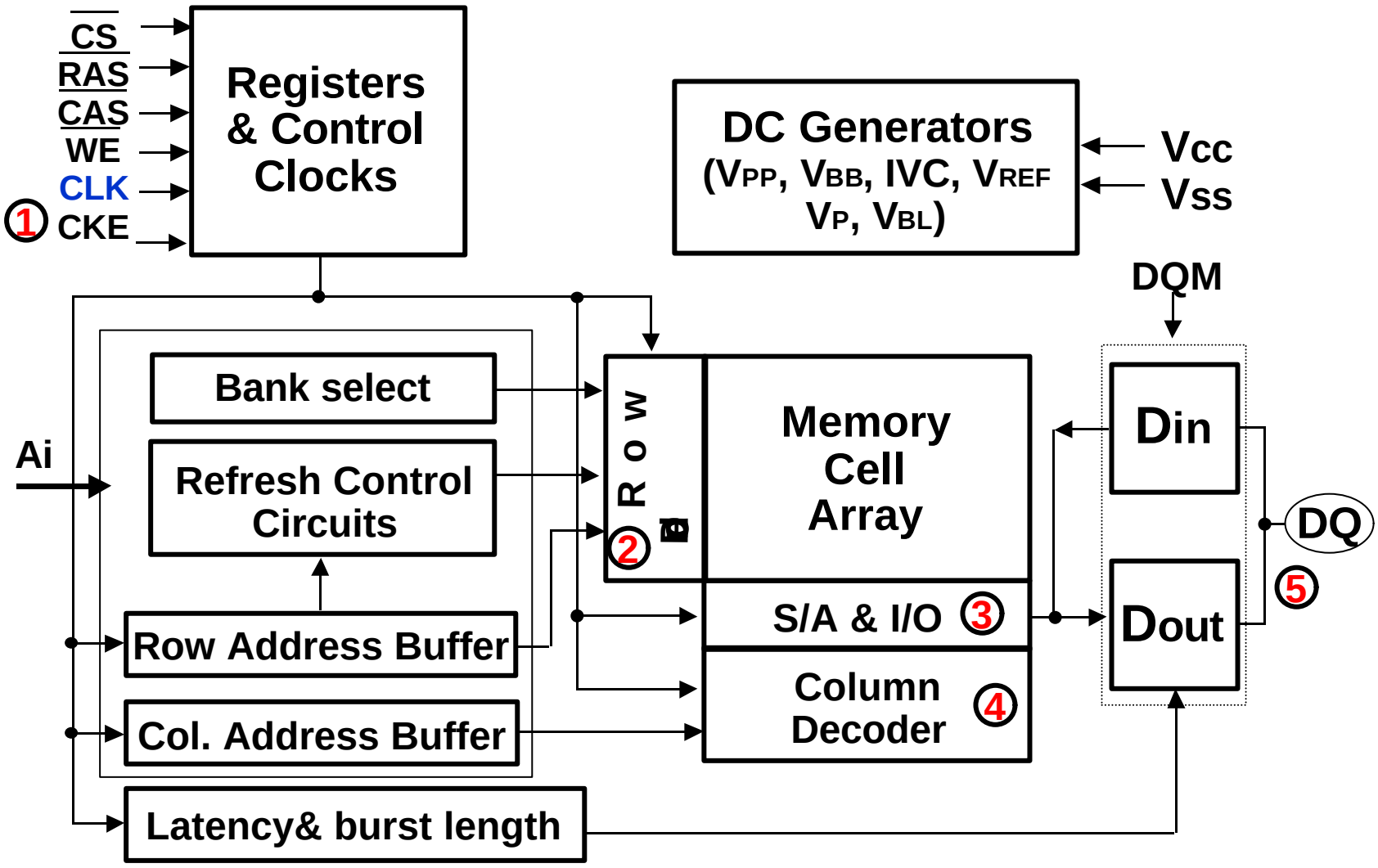
Memory Power Aspect

- DRAM: 0.20 ~ 1.40 W/chip
- SRAM: 0.75 ~ 1.25 W/chip
- NVM: 0.01 ~ 0.10 W/chip

DRAM Introduction & Chip Operation

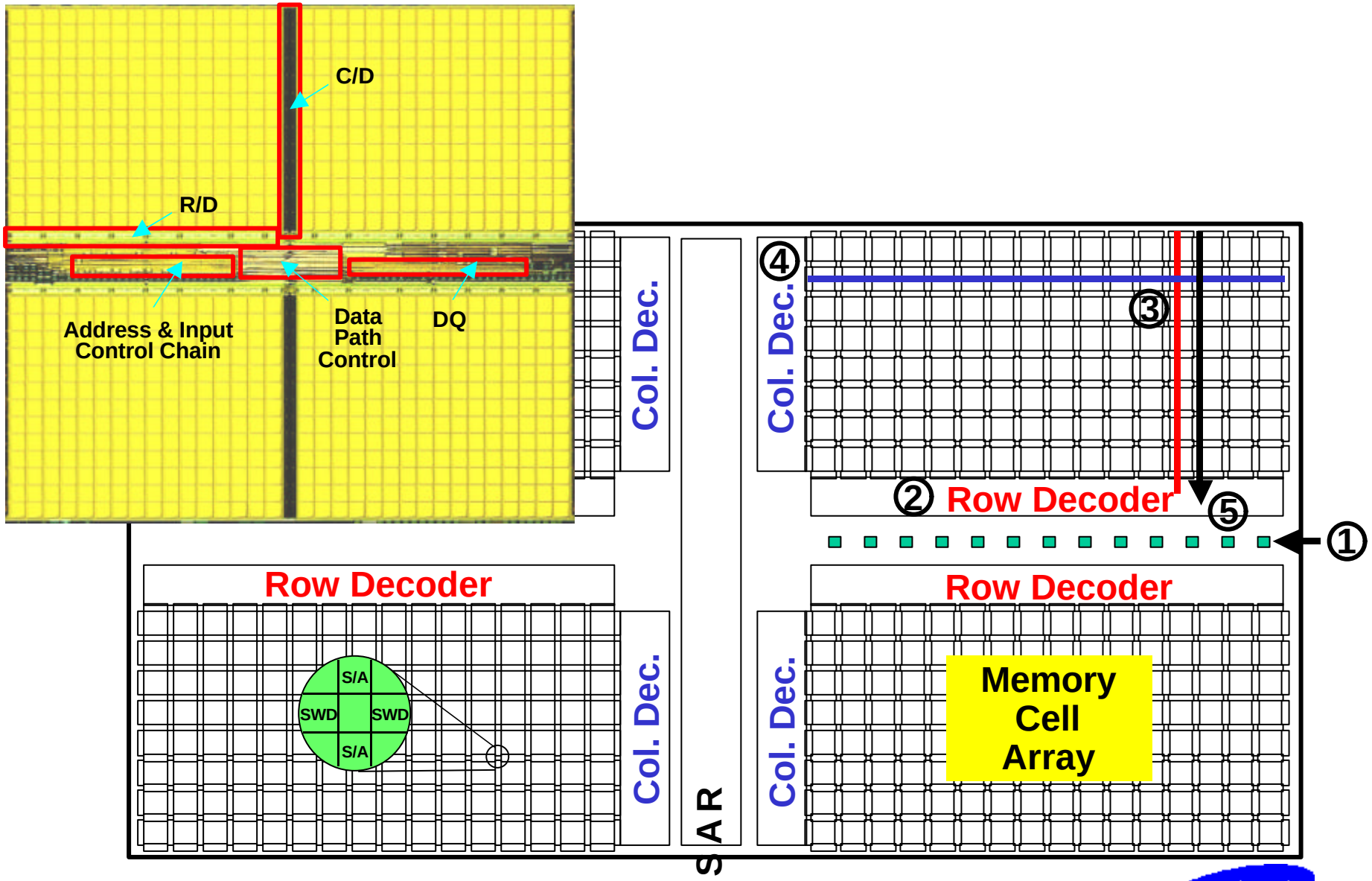
SAMSUNG ELECTRONICS

Functional Block Diagram of SDRAM



SAMSUNG ELECTRONICS

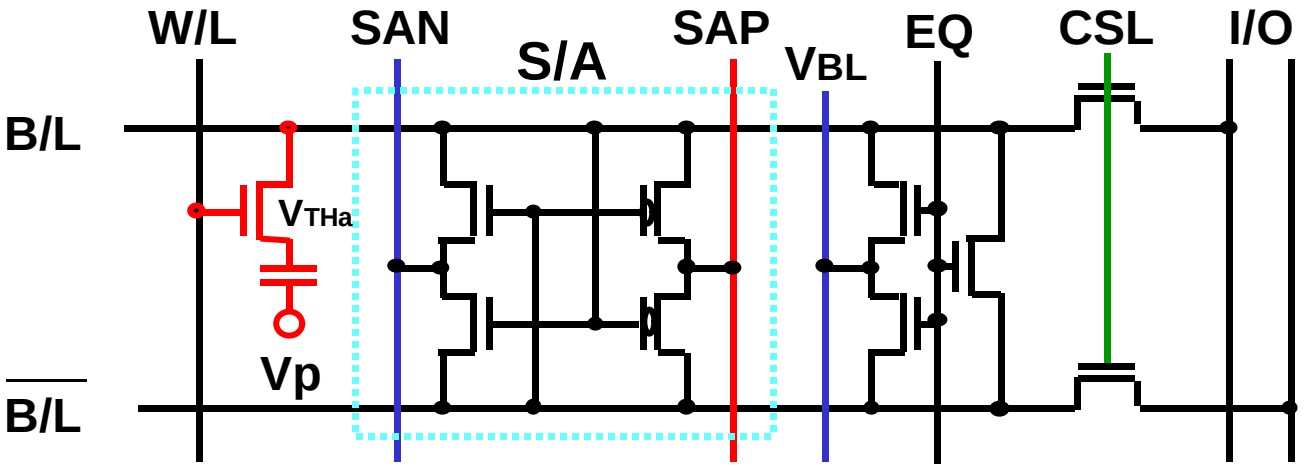
DRAM Chip Architecture & Operation



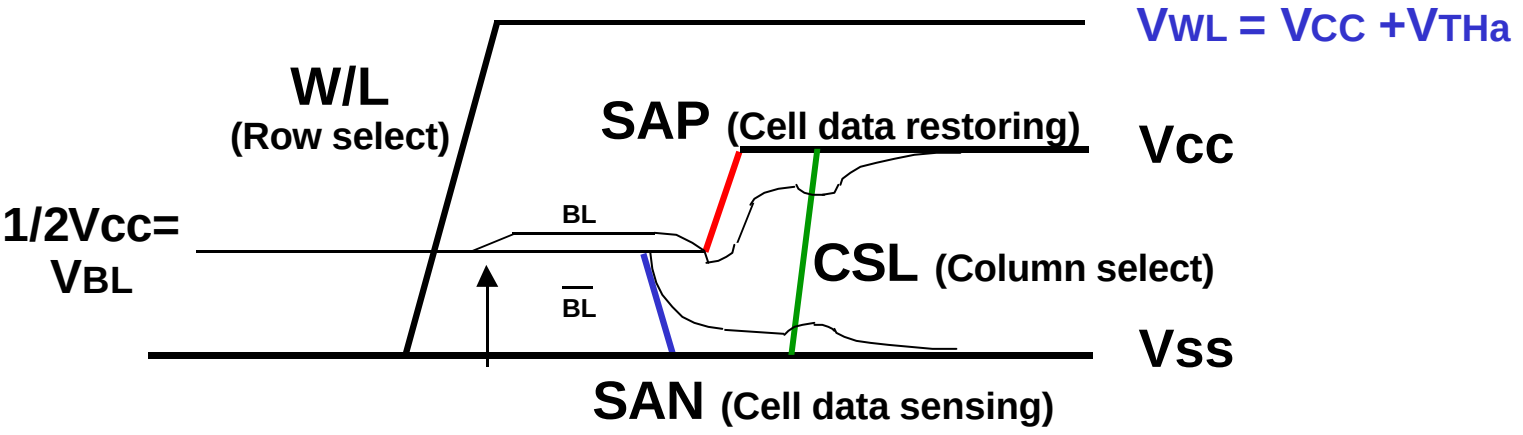
SAMSUNG ELECTRONICS

DRAM Sensing Operation

1/2Vcc sensing scheme



Timing Diagram (for cell data = 1)



SAMSUNG ELECTRONICS

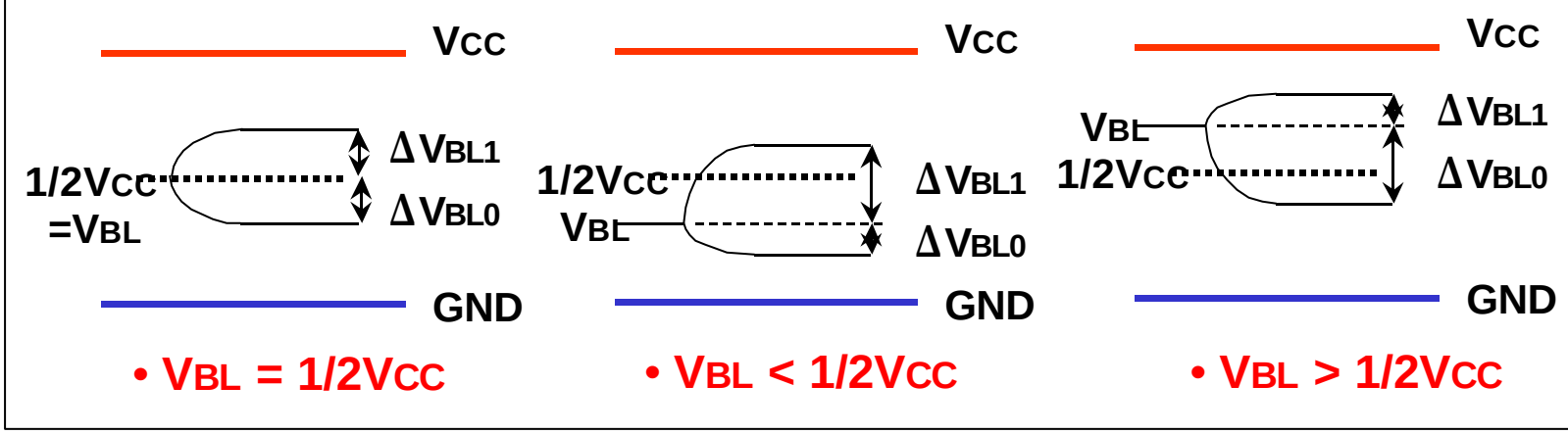
Sensing Margin of DRAM

Sensing margin: Charge conservation law

- **High sensing margin (Data 1=Vcc):**
  - $\Delta V_{BL1}=(V_{Cell}-V_{BL})/(1+C_B/C_S) =(V_{CC}-V_{BL})/(1+C_B/C_S)$

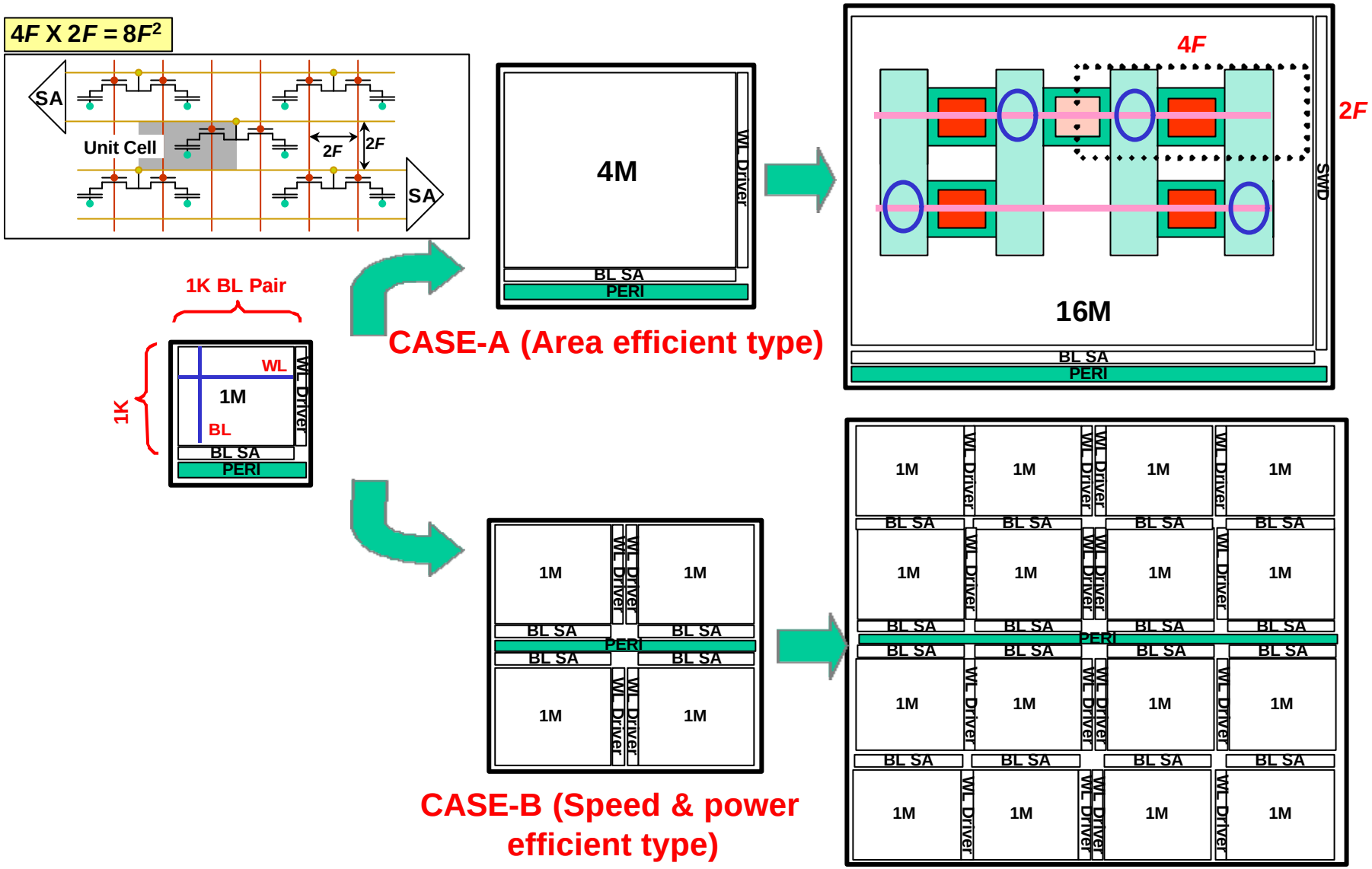
- **Low sensing margin (Data 0=GND):**
  - $\Delta V_{BL0}=V_{BL}/(1+C_B/C_S)$

V_{BL} Level에 따른 Sensing Margin 변화



SAMSUNG ELECTRONICS

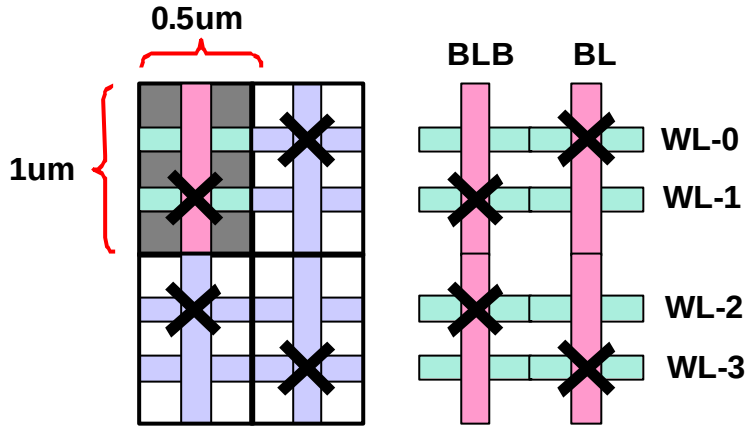
Chip Architecture Example: Folded BL



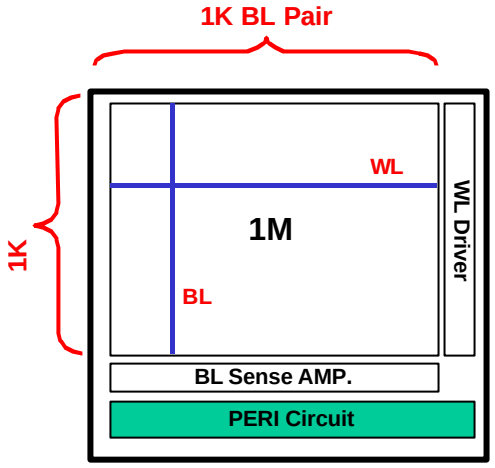
SAMSUNG ELECTRONICS

Chip Architecture Example-1

1. 1M DRAM 구성의 예 ($8F^2$, F=0.25um)



[4-CELL 구성]



[1M DRAM 구성]

1) Chip Size

X축	Y축
CELL ARRAY =0.5umx1KPair = 1.0mm	CELL ARRAY = 1um x 0.5K = 0.5mm
WL Driver = 50um	BL Sense AMP. = 50um
	Peri Circuit = 450um
Total = 1.05mm	Total = 1.0mm

= 1.05mm x 1.0mm = 1.05mm^2

2) Cell Efficiency

= [(1.0mm x 0.5mm) / (1.05mm x 1.0mm)] x 100 = 47.6%

SAMSUNG ELECTRONICS

Chip Architecture Example-2

3) Word Line RC Estimation (1KCell/WL)

WL 저항	WL cap.
- 1Cell당 WL 저항 : 15 ohm	- 1Cell당 WL CAP : 0.3fF
- WL 방향 CELL Unit 수 : 2K	- WL 방향 CELL Unit 수 : 2K
- Total 저항 = 30K ohm	- Total Cap =0.6pF

- WL RC time constant (τ) = 30K ohm x 0.6pF = 18ns

4) Delta VBL Estimation (512Cell/BL)

- Cell Cap(CS) : 0.03pF	- ARRAY 전압 (VCCA) : 2.0V
- 1Cell당 BL Cap : 0.5fF	- BL Precharege 전압 (VBL) : 1.0V
- BL 방향 CELL Unit 수 : 0.5K	- BL Active 주기 : 100ns
- Total BL Cap(CB) : 0.25pF	

- Delta VBL (DATA'1) = (VCCA - VBL) / (1 + CB/CS)
  = (2.0V – 1.0V) / (1 + 0.25pF/0.03pF)
  = 107mV

5) BL Sensing Current Estimation

- BL Current = (CB x VBL x 1K BL Pair) / BL Active 주기
  = (0.25pF x 1.0V x 1K) / 100ns
  = 2.5mA

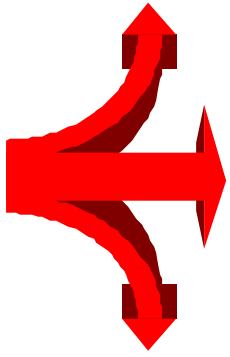
DRAM Technology Trend

- High Density Approach
- High Speed Approach
- Low Power Approach

Memory Technology Innovation

Historic 3 Momentum Words for Memory:

Density, Speed, Power



High Bit Density (~1.0Gb/cm^2)

- Advanced Process Technology:
- 2-D & 3-D cell approaches
- Stacking chip/package solutions

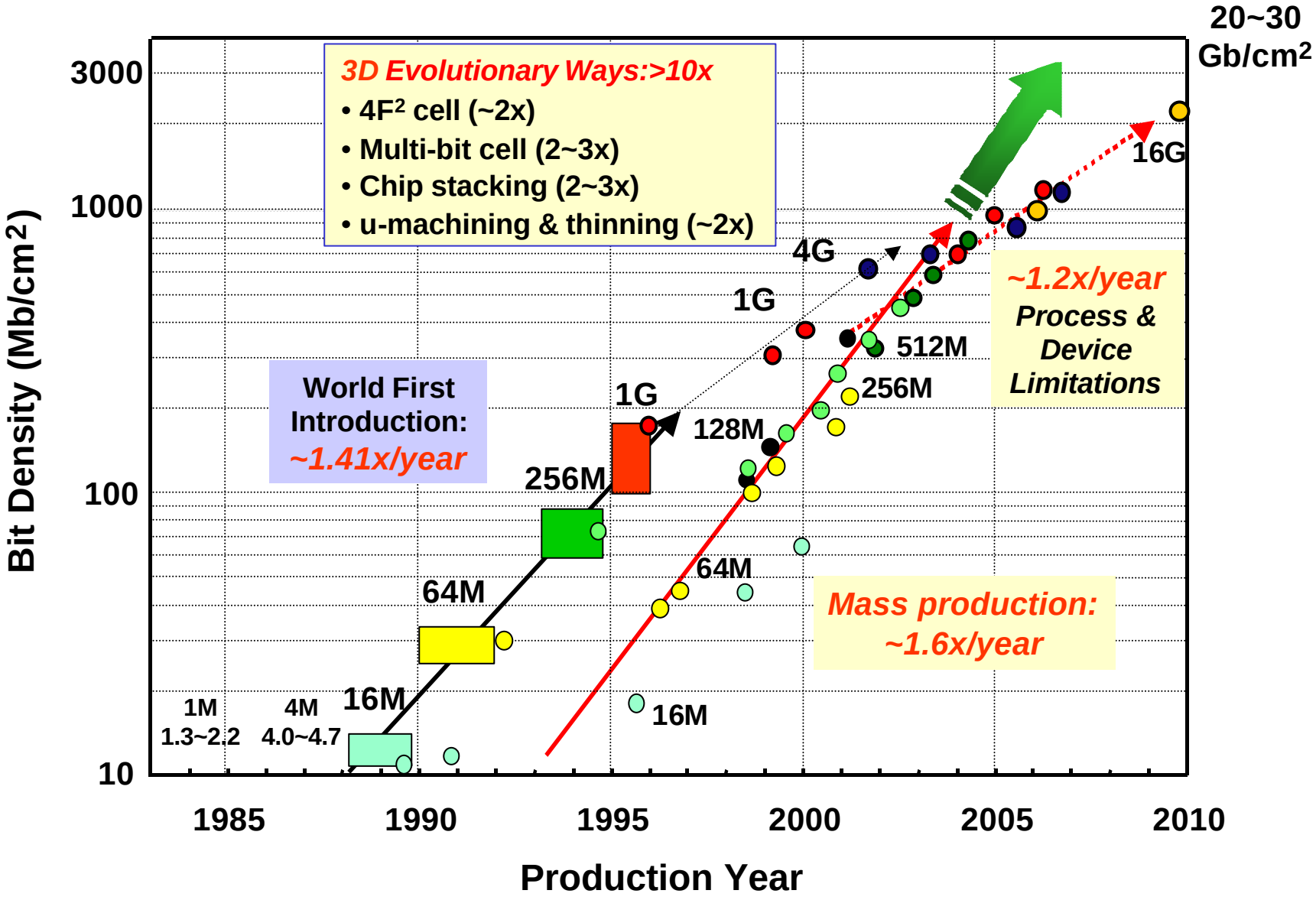
High Speed (tRC= 20~60ns, I/O=200~1000MHz)

- Improved latency with array partitioning
- High BW with new small swing I/O interface schemes

Low Power (2.5~1.8V, Standby<0.2mW, Active <1.4W)

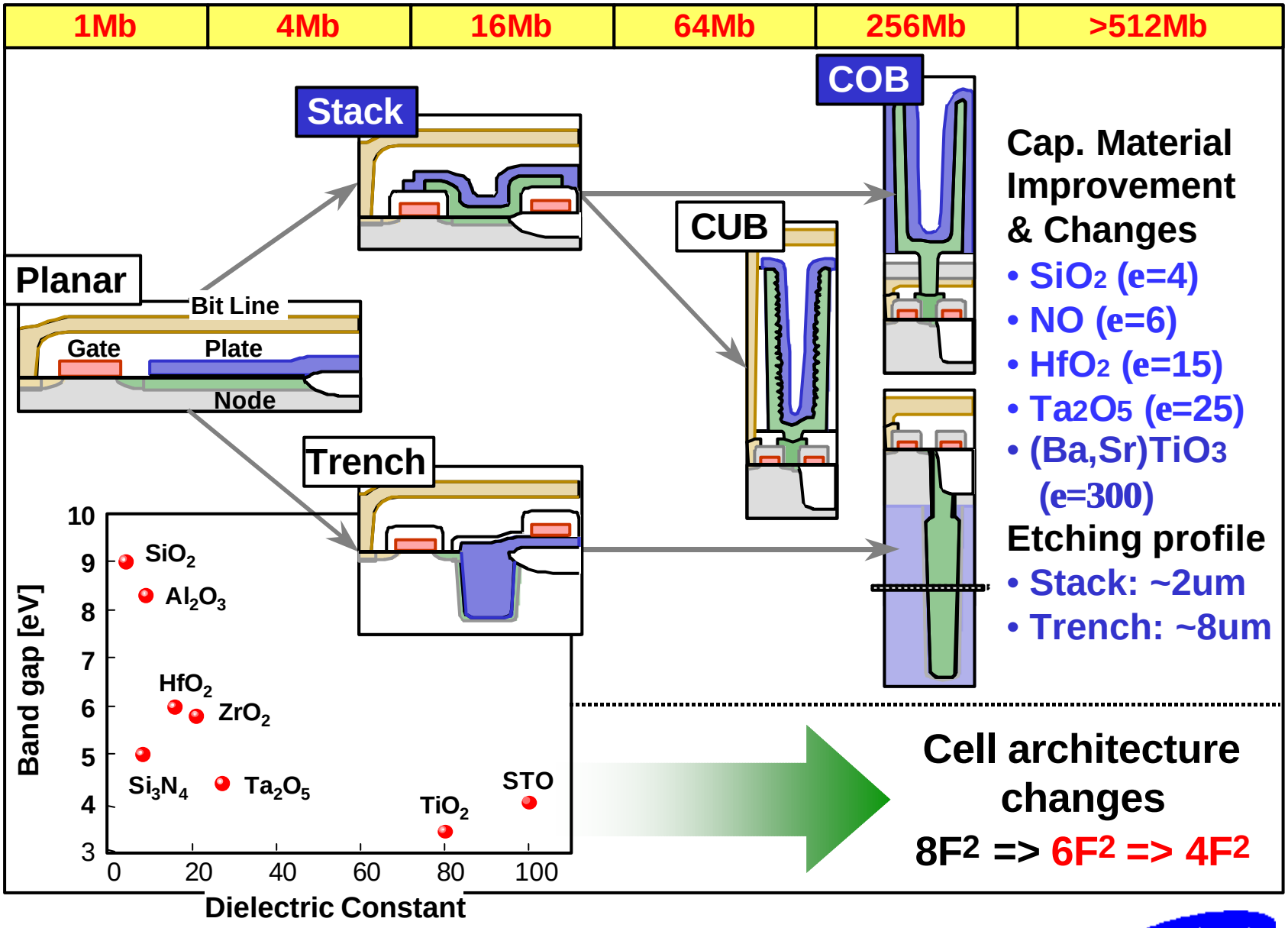
- Voltage reduction with device scaling
- Low standby power circuit schemes

DRAM Bit Density Increase Trend (1)



SAMSUNG ELECTRONICS

Trend of DRAM Cell Structure

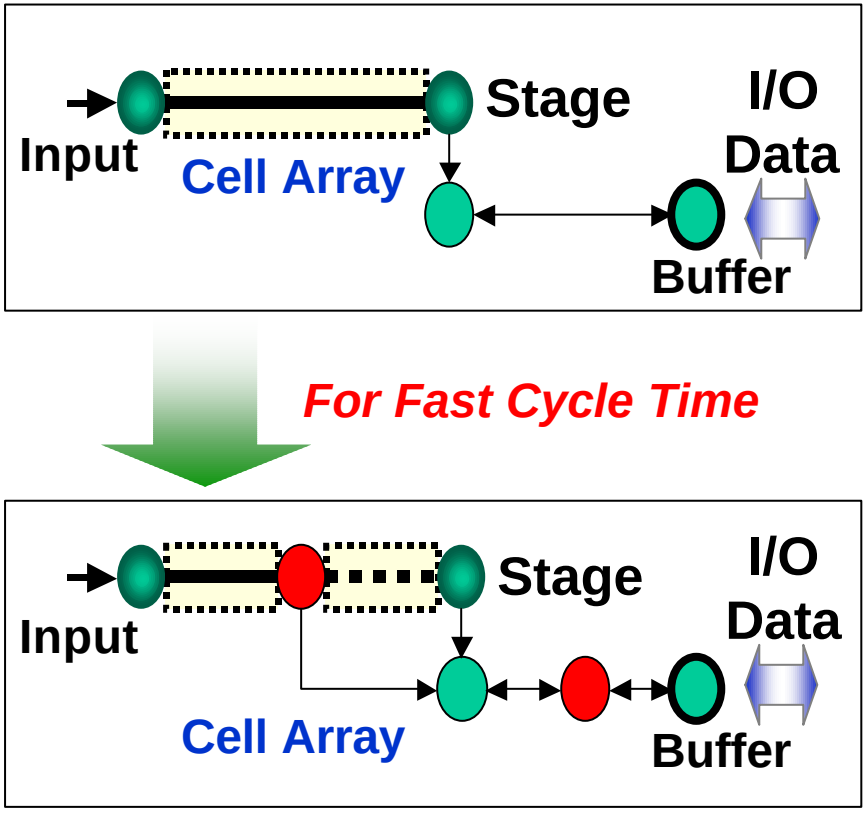


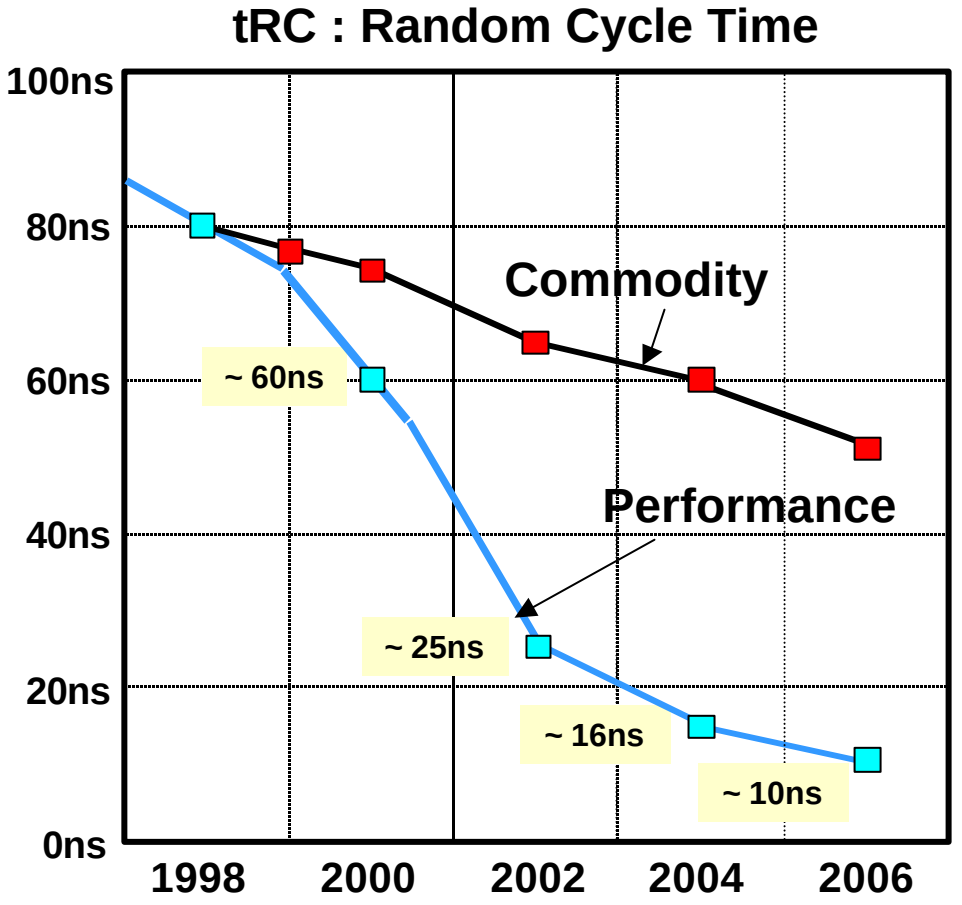
SAMSUNG ELECTRONICS

DRAM Technology Trend (2)

High Speed Aspect (Latency)

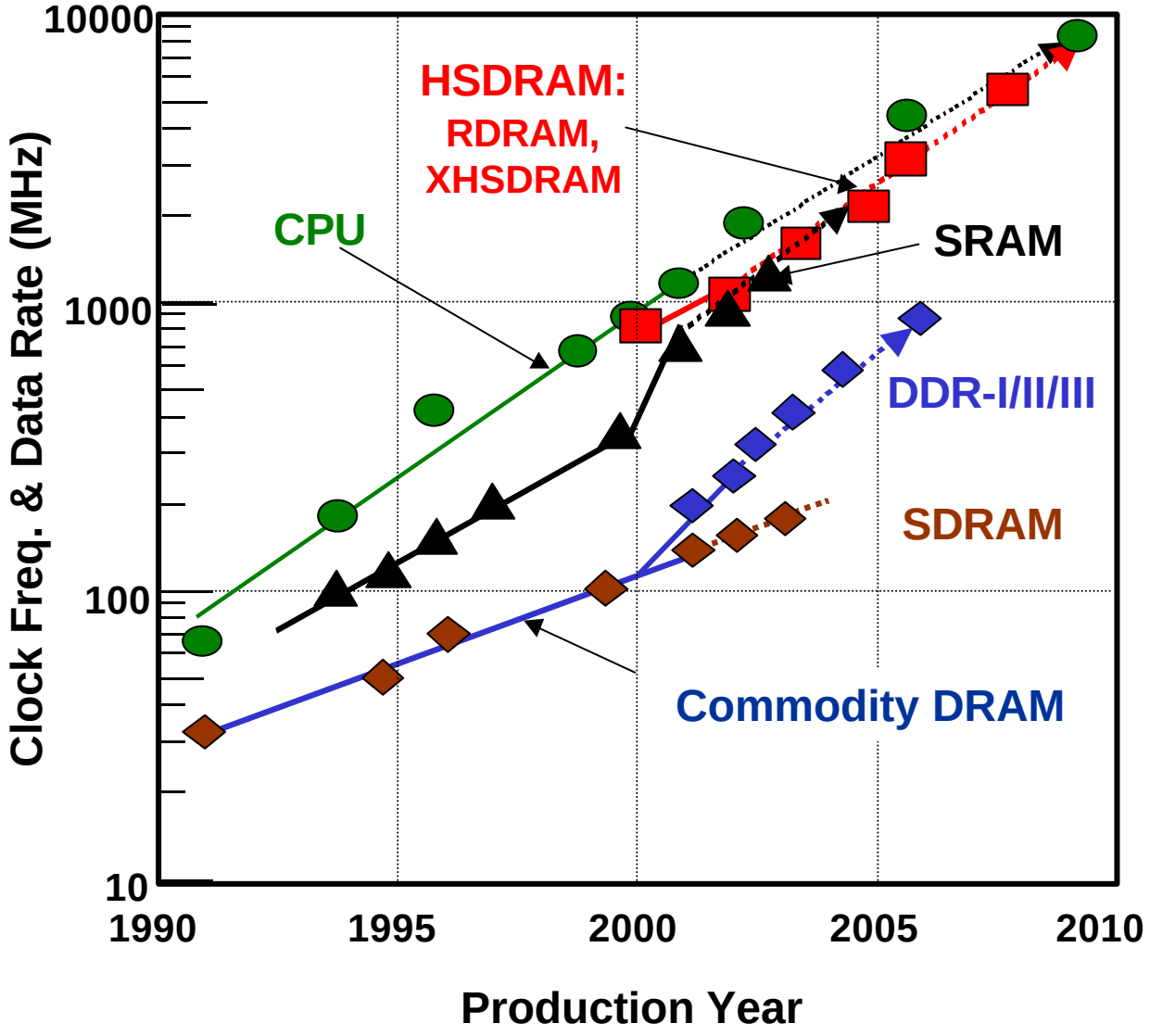
- *Array-Partitioning (& Multi-Stage) Methods*





SAMSUNG ELECTRONICS

Trend of Memory Data Transfer Rate

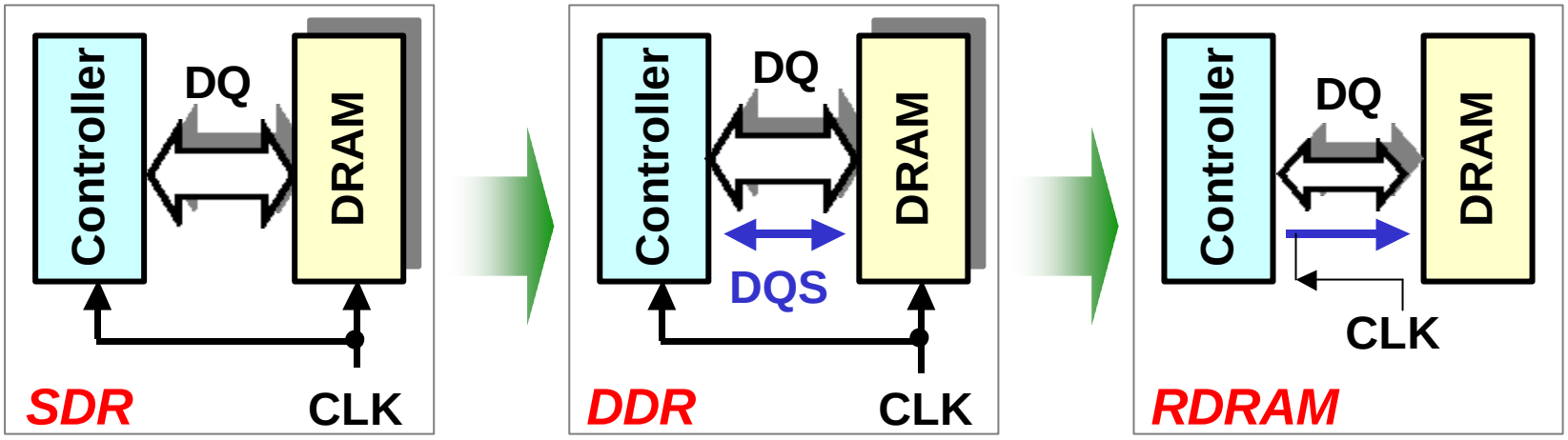


Achievement Ways

- Advanced process Technology
- High speed logic
- New I/O schemes
  - DDR, QDR, ODR
  - Sim. Bidirectional
- Robust signaling
- Small channel skew
- Tight pin parasitic

SAMSUNG ELECTRONICS

System Signaling Trend (Skew, 3D)



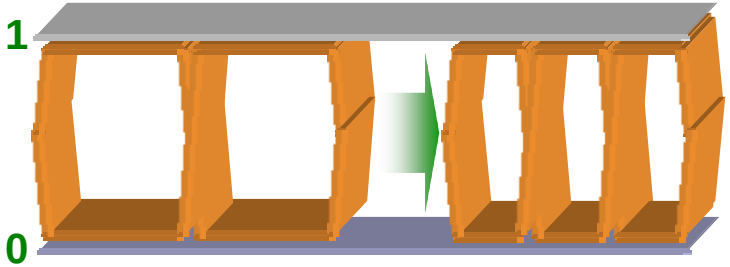
Large CLK-DQ Skew

Small CLK-DQ Skew with strobe scheme

"Zero" CLK-DQ Skew with synchronization

2-D Data Transfer

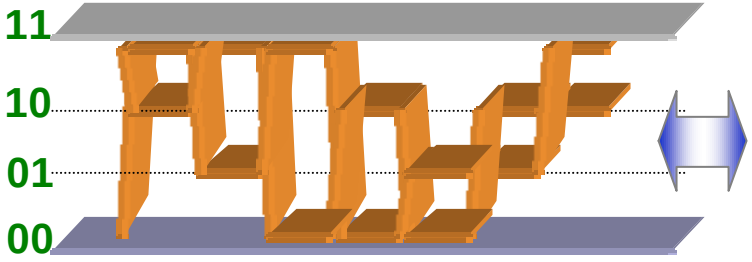
- *SBT (Single-Bit data Transfer)*
  SDR => DDR => QDR =>ODR



3-D Data Transfer

- *MBT (Multi-Bit Transfer: PAM)*
- *SBDT (Sim. Bi-Directional)*

2bit case



SAMSUNG ELECTRONICS

Reduction of Power Consumption

Power Consumption Reduction Ways

- Use of Advanced Process Technology
  - Shrinkage: 0.72x ~0.84x/Year
- Adoption of Lower Operating Voltage
  - 3.3V => 2.5V => 1.8V => 1.5V => 1.2V => 1.0V
  - Sensitivity: ~85mA/0.5V (RDRAM)
- Use of Several Power-Efficient Circuit Techniques
  - Low power DLL and optimized clock tree
  - Shared circuit/logic scheme
  - Small swing I/O scheme
    - GTL (Open-Drain) type: Reduced loading
  - Power-Efficient logic:
    - CPTL: complementary pass transistor logic
    - DSCVSL: differ. split level cascode voltage switch logic
  - Adiabatic circuit techniques

Operating Voltage Migration Trend

Lower Voltage for Low Power Consumption

- Max. power consumption for HSDRAM (< ~1.0W)
- Low standby current (<100uA)
- Reliability: Hot-carrier stress & max. oxide field

DRAM

Year	2002	2004	2006	2008	2010
DR	~0.13um	~0.10um	~0.08um	~0.07um	~0.055um
Density	256M	512M~1Gb	1~2Gb	2~4Gb	4~8Gb
Voltage (Intro.)	~2.5V	~1.8V	1.5~1.35V	1.2~1.35V	1.0~0.9V

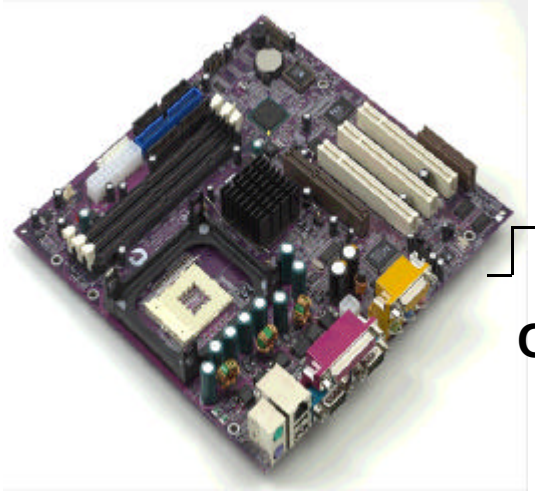
Logic (CPU+ASIC)

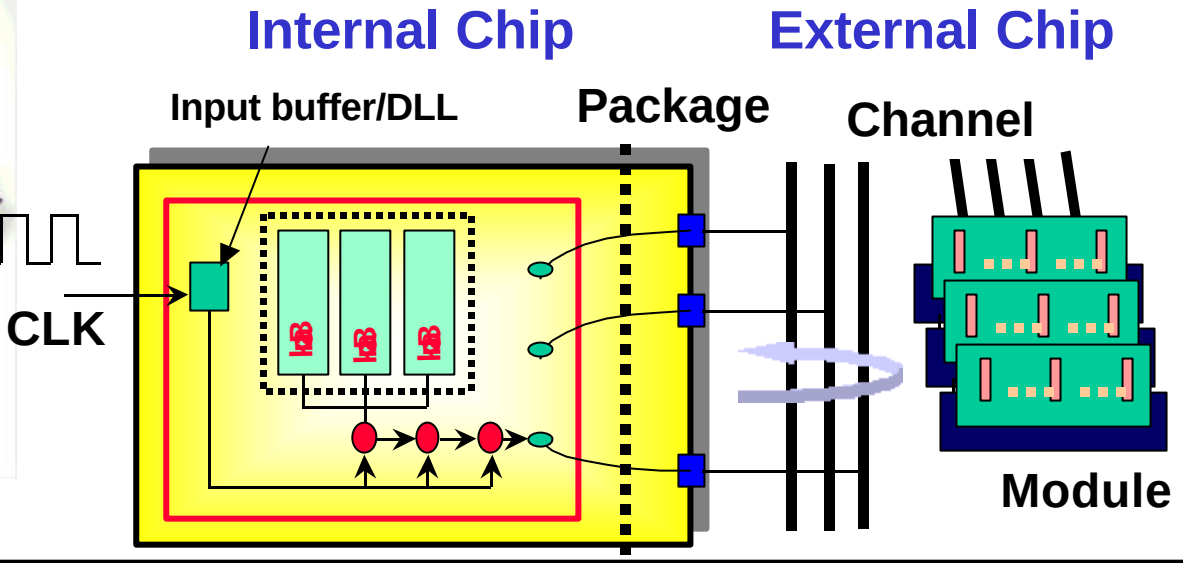
Year	2002	2004	2006	2008	2010
DR (L)	~0.13um	~0.09um	~0.07um	~0.06um	~0.045um
Voltage	1.2~1.5V	0.9~1.2V	0.7~1.0V	0.6~0.9V	0.5~0.6V

Challenges for High Performance DRAM

SAMSUNG ELECTRONICS

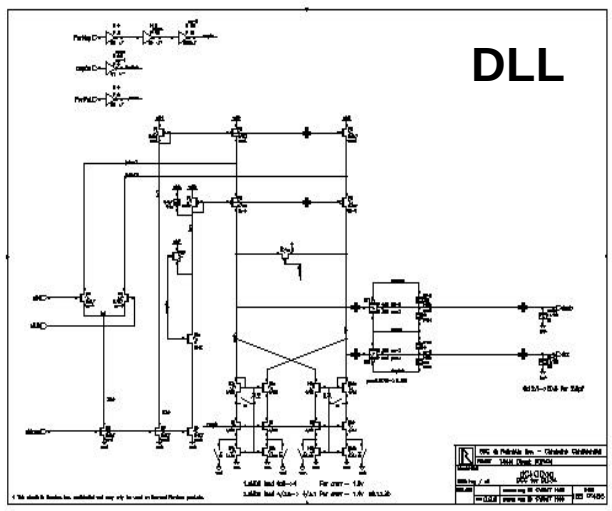
Memory System Overview & Challenges

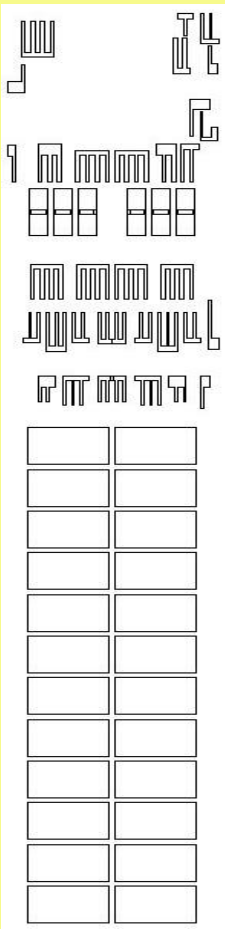




	Chip	Package	Channel
Goals	High speed, Low latency Low power, High density	Low Parasitic High Thermal dissipation	High Bandwidth Low power Good signal integrity
Challenges	High speed circuits (DLL, I/O buffer) Low voltage design, Low jitter/skew PVT variation, Tester calibration	RLC Parasitics Reliability	Skew reduction PCB channel design Impedance matching
Solutions	PVT insensitive design Multi-array partitioning & Multi-stage I/O architecture Adaptive I/O, On chip-calibration Advanced Technology (<0.1 ㎛)	u-BGA WL BGA FC BGA MOST	Low swing & High speed signaling: SSTL, RSL, HSTL P2P communication

Design Methodology: Process Variations



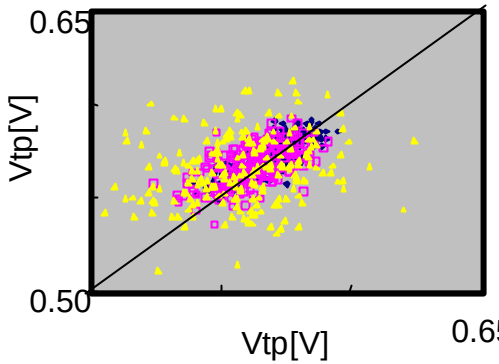


Statistical Analysis

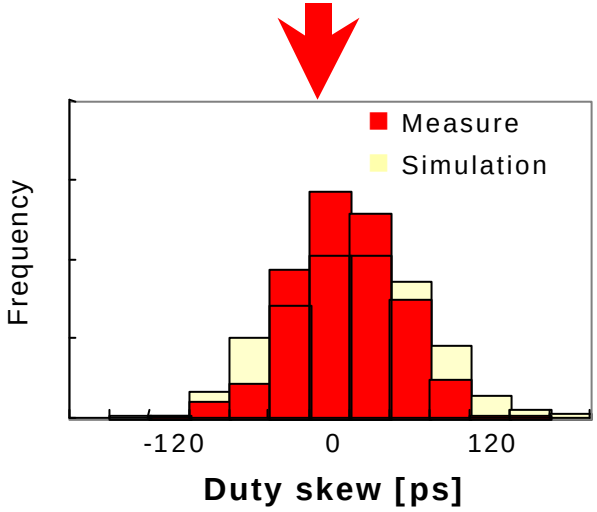
- Monte Carlo Simulation
- Sensitivity Analysis

CAD Tool Development

- Statistical parameter generation
- OPC Technique



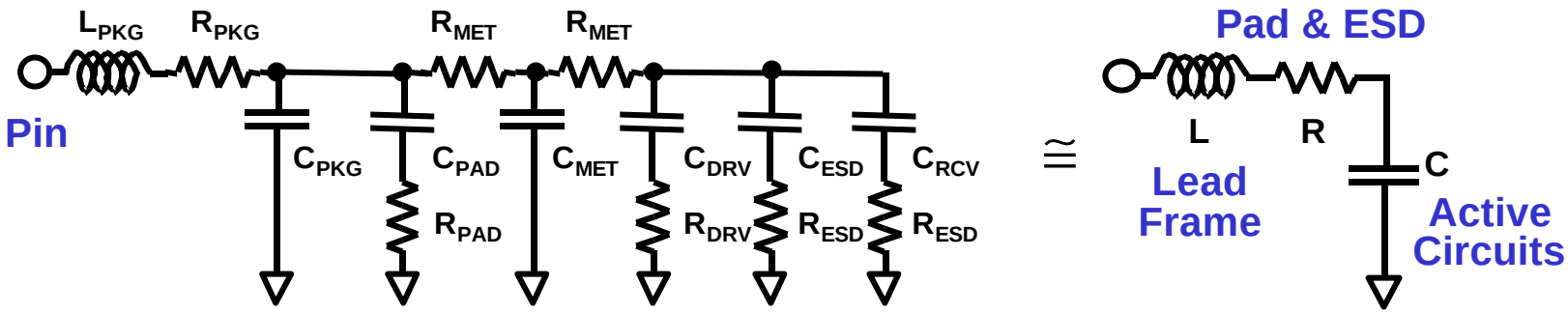
Vth mismatching of Paired PMOS Transistor



SAMSUNG ELECTRONICS

High Speed Approach-Package

Pin Parasitic Modeling and Optimization



- **Pin Parasitics:**
  - **RLC affects signal loss, input signal ringing, voltage & timing margins, impedance, & propagation delay**

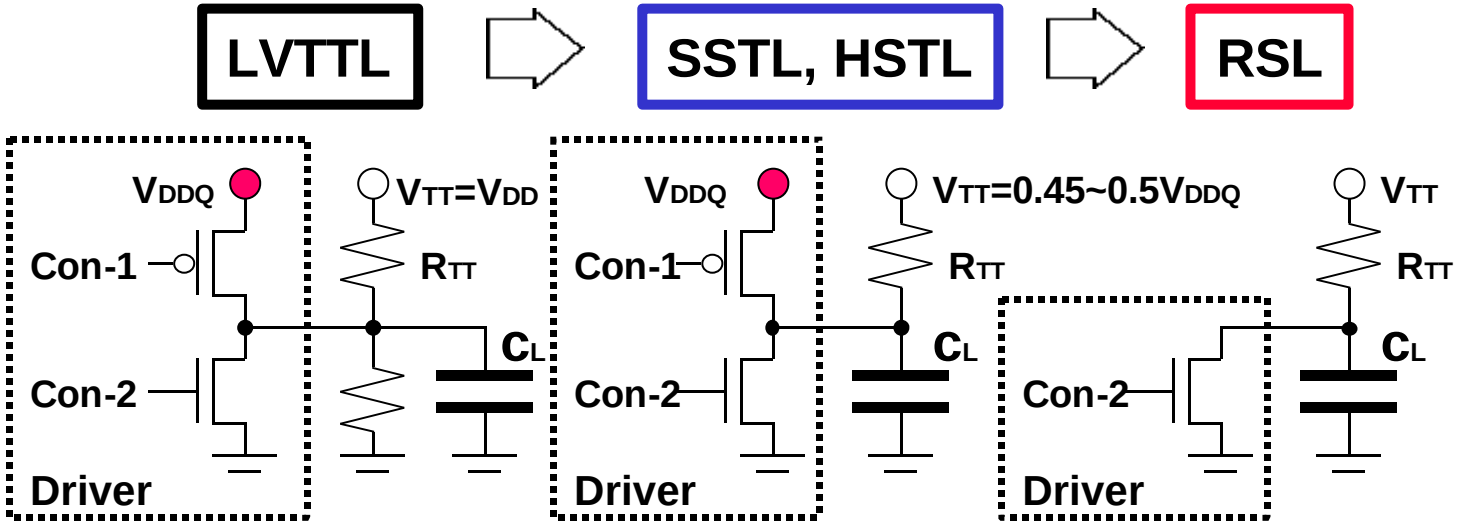
Parasitic Items	SDRAM (100~150MHz)	DDR (200~400MHz)	RDRAM (800~1000MHz)	HSDRAM (2~4GHz)
	CLK~DQ	CLK~DQ	CLK~DQ	CLK~DQ
Rin (Ω)	14~17	14~19	8~9	4~7
Lin (nH)	3~4.5	2.4~4.0	1.0~2.5	1.0~2.0
Cin (pF)	3.7~5.6	2.9~4.4	~2.2	~1.5
Δ Cin (pF)	1.9	1.5	< 0.06	< 0.04

SAMSUNG ELECTRONICS

I/O Interface Schemes

Requirements for Future High Speed Interface:

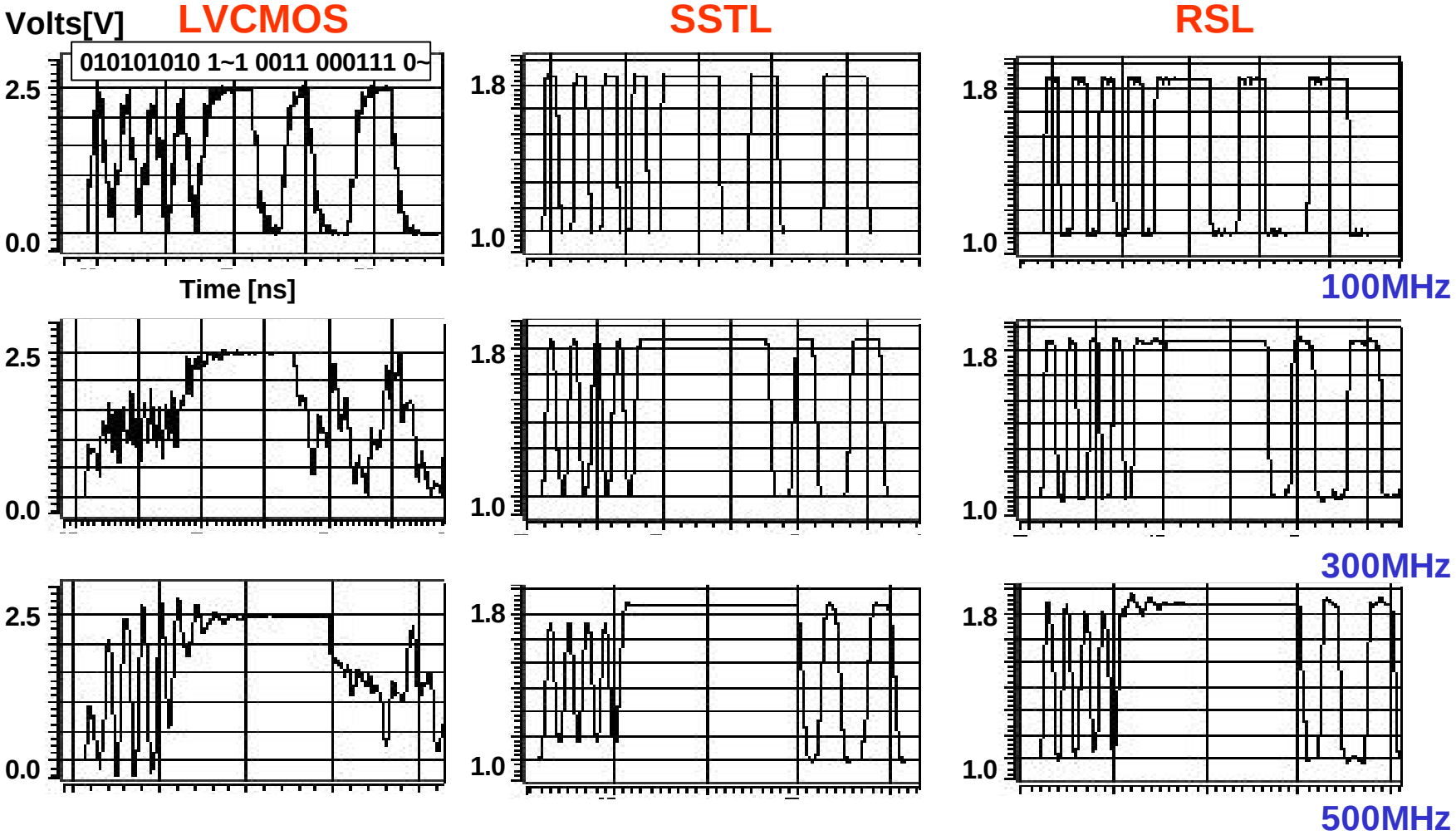
- High Speed Data Transfer Rate: >200Mbps
- Good Signal Integrity
- Small swing scheme: 2.0V - 1.0V
- Low Power Consumption: Low V_{DDQ} from 3.3V -to-1.8V



SAMSUNG ELECTRONICS

I/O Interface Schemes-2

High Speed I/O Interface Implementation for Good Signal Integrity

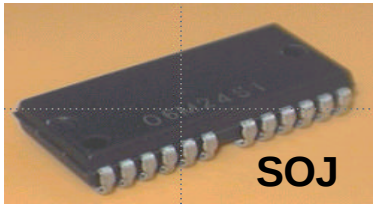


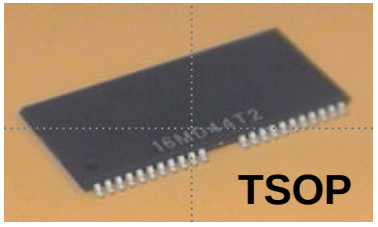
SAMSUNG ELECTRONICS

Package: Technology Trend

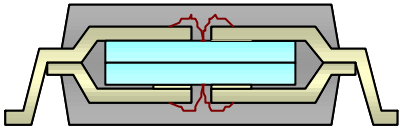
Future Trend: High Density & High Speed

- **High Density** (Large memory size/volume) & **SIP**
  - Vertical stacking: PKG Stack, DDP
  - Horizontal placing: MCP
- **High Speed** (Small dimension & low parasitic)
  - Chip scale package: BGA, FBGA
  - Low parasitic package: u-BGA, WLCSP

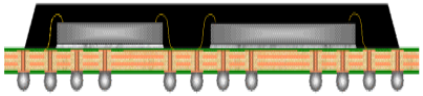




Stacked Package

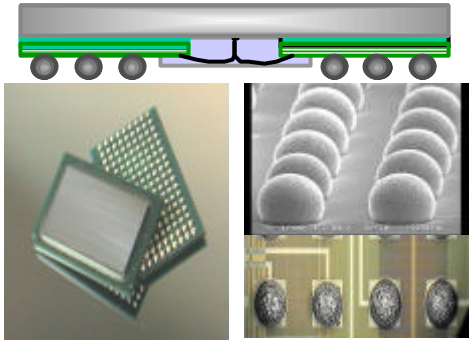


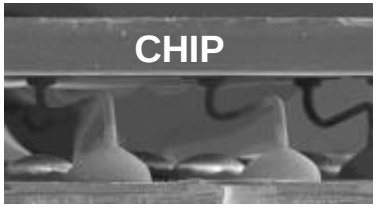
DDP



MCP

BGA/CSP



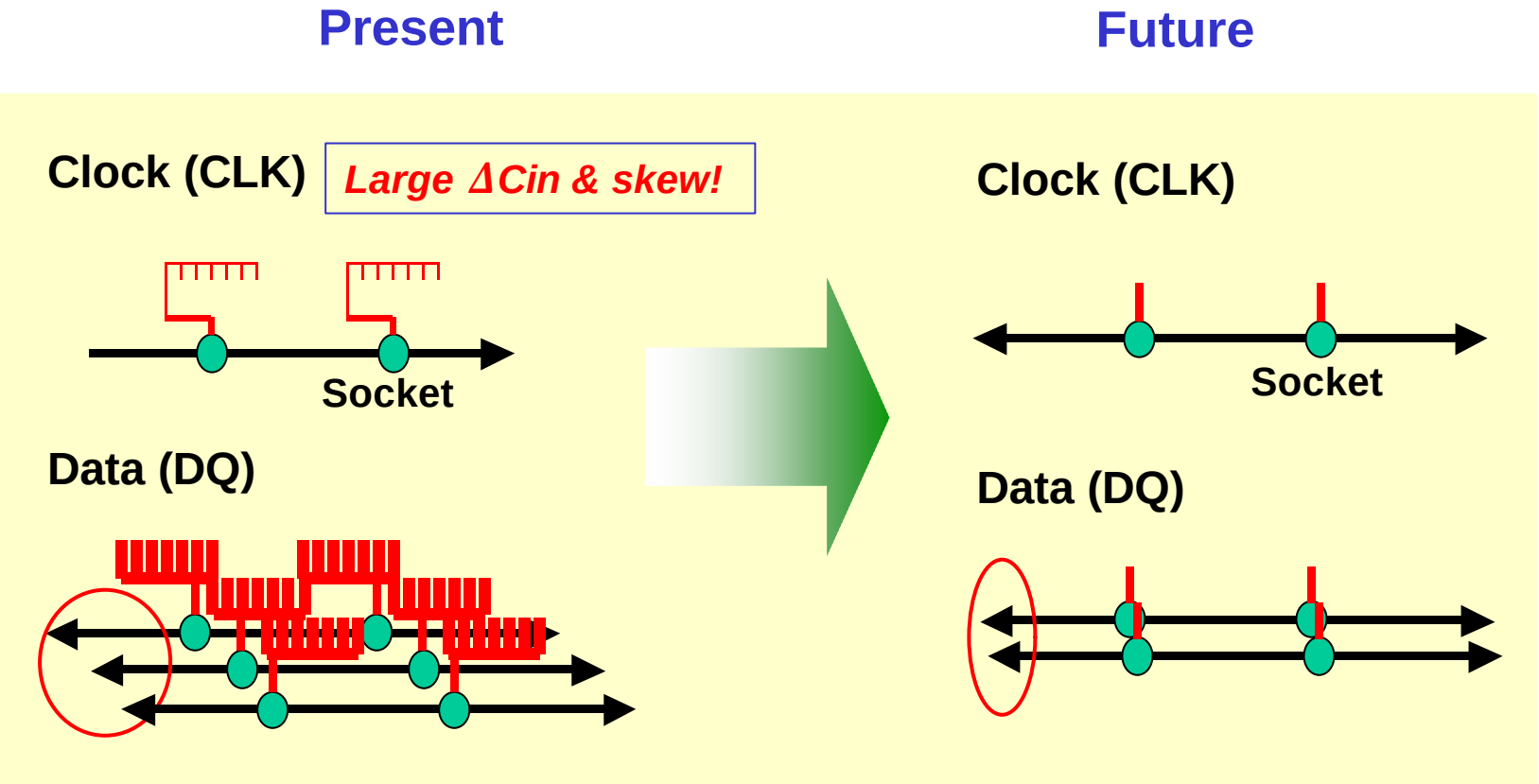


- Low speed
- Low packing density

- High speed
- High packing density

SAMSUNG ELECTRONICS

System Trend: Reduction of Skew & Pin-Counts

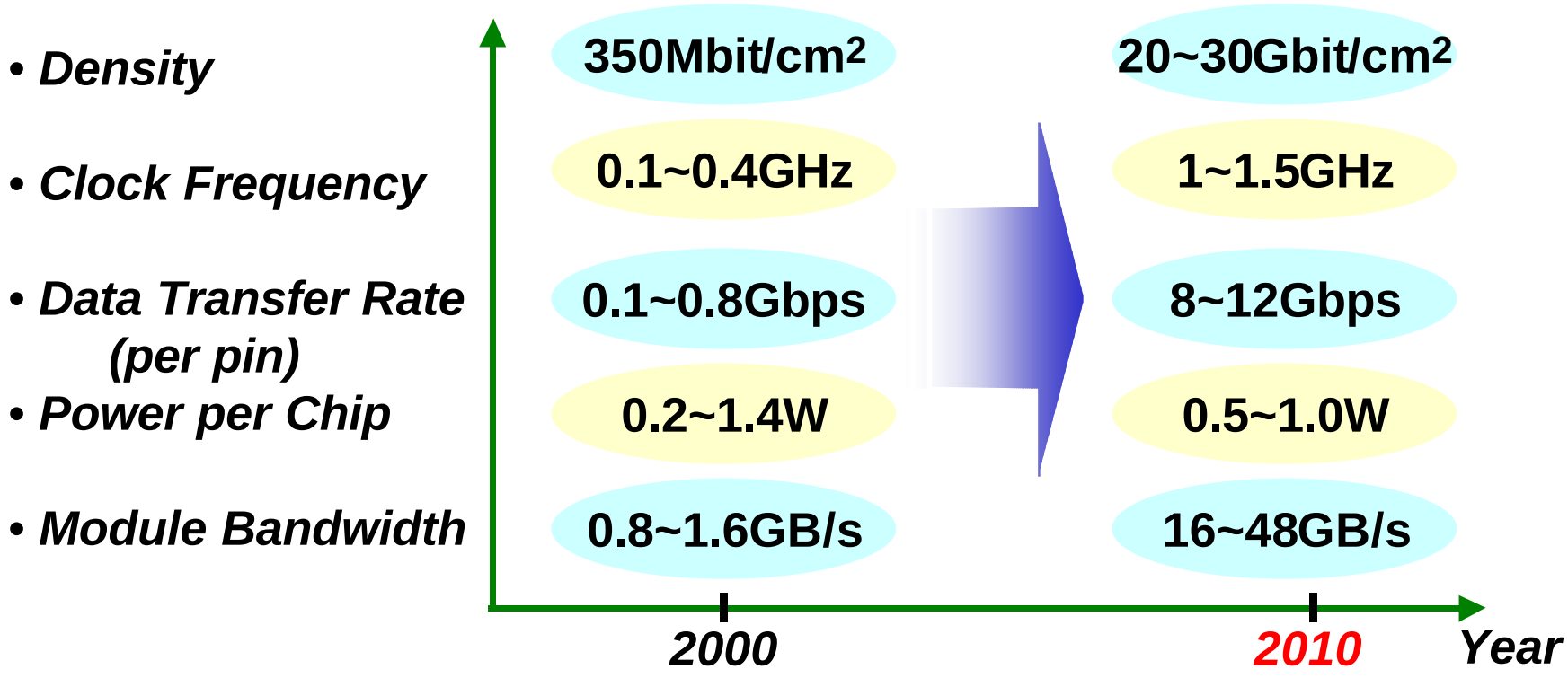


- Loading Difference
- Large No. of pins

SAMSUNG ELECTRONICS

Conclusions

Future Memory Performance Projection



DRAM will continuously evolved to realize high performance GigaHz memory systems with improved existing technologies (for density, speed, and power) and application-specific memories to closely meet the customers' demand.

SAMSUNG ELECTRONICS

Emerging Memory for Year of 2005+

One commodity memory is widely used for most major systems

~2000
Universal Standard Memory

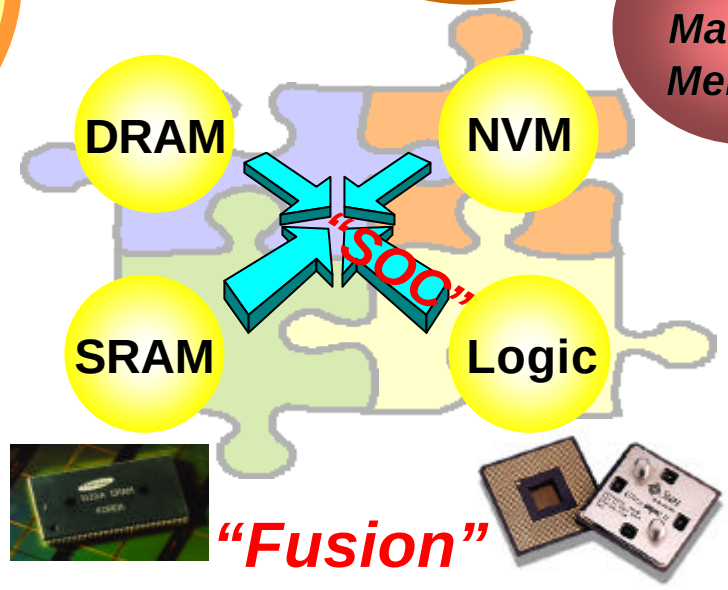
Each specific application requires special memory solution

~2005
System Solution Memory

Total Solution

2005+
Fusion Memory
(DRAM + SRAM + FLASH + Logic)

New Material Memory



"Fusion"

SAMSUNG ELECTRONICS

Conclusions

In the future, more evolutionary and/or revolutionary technical approaches will actively take place to overcome several challenging issues in high performance memory operations.

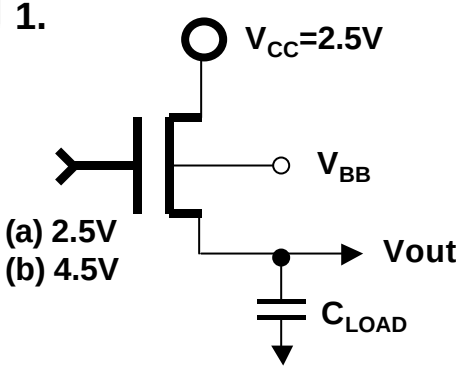
For successful integration of high performance memory systems, aspects of off-chip as well as on-chip technologies such as the package and module issues must be addressed to achieve the requirements for low parasitics, good signal integrity, and high bandwidth with small form factor.

Many technical approaches can be employed for the realization of diversified high performance memories for total solutions:

- *High density approaches*
- *High speed I/O interface schemes*
- *Low power consumption ways*
- *New material memory development*

Homework (DRAM Design)

문제 1.

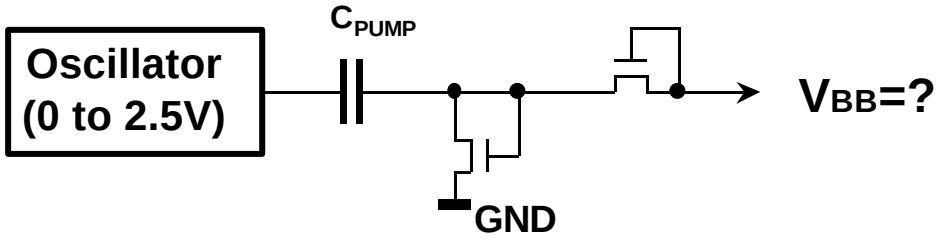


옆의 그림과 같이 NMOS Transistor의 Gate에 (a) V_G=2.5V, (b) V_G=4.5V가 인가될 때, 각각의 경우 Vout의 maximum voltage를 구해 보시오.

사용 Parameters:
V_{TO} (= 1V@V_{BB}=0V), $2\Phi_f$=0.8V, g (body effect 고려 상수)=0.7 $V^{1/2}$
V_{BB}=-1V, $V_T = V_{T0} + g\left(\sqrt{|V_{BS}| + 2\Phi_f} - \sqrt{2\Phi_f}\right)$

문제 2. 1 Gbit (x1) Cell Array를 갖는 DRAM을 설계하려고 한다.
(a) Row(X), Column(Y)의 Address 숫자를 같이 한다면 X,(Y) address pin의 개수는?
(b) 또, Cell의 leakage current가 1pA/cell 이고, Sense Amplifier의 offset voltage (threshold voltage의 차이=0.1V)를 고려할 때 Cell을 Refresh를 해 주어야 하는 최소시간 또는 주기를 구하시오.
가정: Vcc=2.5V, Cs (Cell cap.) = 20fF, Cb (bit line cap.) = 180fF
1/2 Vcc Bitline sensing scheme, Q (charge) = C x V = I x t 로 단순 고려.

문제 3. 다음은 Conventional N-MOS type의 Negative voltage generator 이다.
아래 회로에서 V_{BB}가 도달 할 수 있는 최소 level은 얼마 입니까?
가정: NMOS Vth = 0.7V (Body Effect 는 고려하지 않음)



SAMSUNG ELECTRONICS